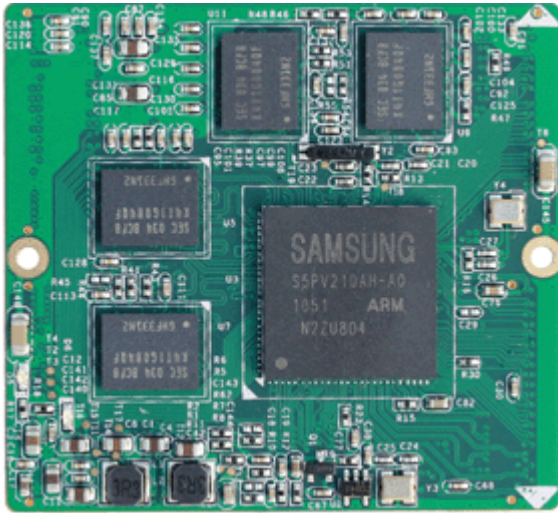
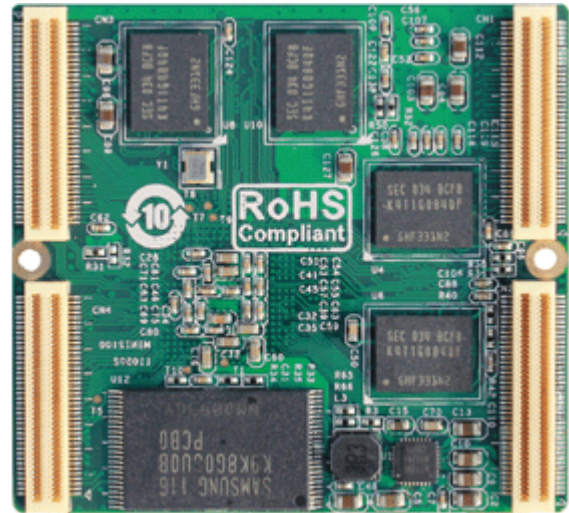


Embest Mini2100 Processor Card



Top-View



Bottom-View

Features

Mechanical Parameters

- Dimensions: 55.2 mm x 50.5 mm (8 layer PCB design)
- Working temperature: 0~70 Celsius
- Humidity Range: 20% ~ 90%
- Power Consumption: 200mA @ 5V

Processor

- Samsung S5PV210 Mobile Application Processor
 - Up to 1-GHz ARM® Cortex™-A8 Core with NEON, also supports 800-MHz operation
 - 32KB I-Cache; 32KB D-Cache; 512KB L2 Cache
 - Onchip 64KB ROM and 96KB SRAM
 - Built-in the programmable PowerVR SGX540 core
 - 2D/3D Graphics Acceleration
 - Multi Format Codec provides encoding and decoding of MPEG-4/H.263/H.264 up to 1080p@30fps and decoding of MPEG-2/VC1 video up to 1080p@30 fps

Memory

- 1GBytes Mobile DDR2, 8-bit
- 1GBytes NAND Flash, 8-bit

Expansion Interfaces and Signals Routed to Pins

- Four 0.5mm space 2*40-pin board-to-board female expansion connectors
 - TFT LCD Interface (support 24/ 18/ 16-bpp parallel RGB Interface LCD)
 - Analog TV interface (support NTSC / PAL)
 - HDMI Digital TV Interface (Supports 480p, 576p, 720p, 1080i, 1080p)
 - 3-channel Camera Interfaces (Supports ITU-R BT 601/656 YCbCr 8-bit, MIPI mode)
 - PCM Audio Interface (Supports three port PCM interface)

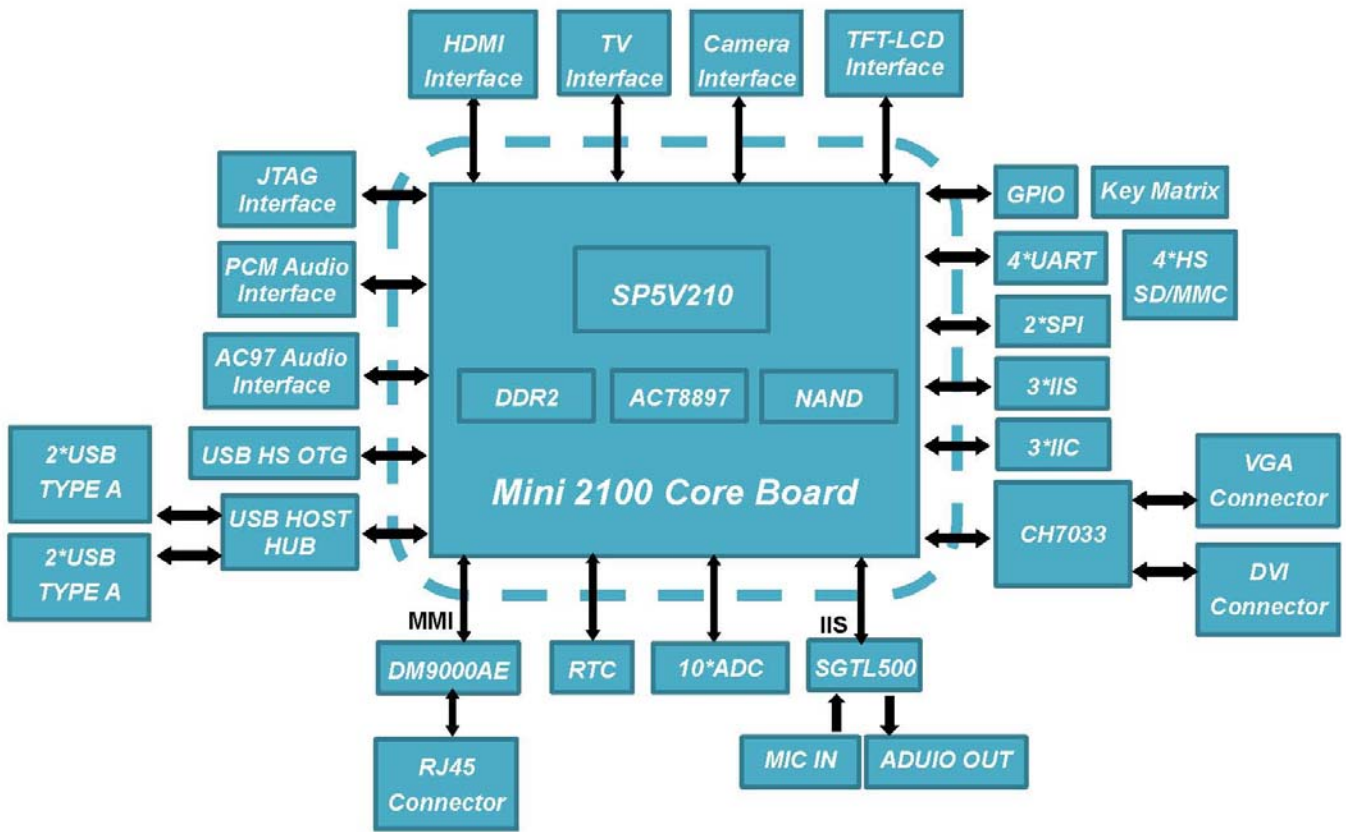
- AC97 Audio Interface (Supports AC97 Full Specification)
- JTAG Debugger Interface
- USB 2.0 OTG (Supports high-speed up to 480 Mbps)
- USB 2.0 Host (Supports high-speed up to 480 Mbps)
- 14*8 Key Matrix support
- 2-channel SPI Interfaces
- 3-channel IIS bus interfaces
- 3-channel IIC bus interfaces
- 4 channel HS-MMC/SD
- 4-channel UART (Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/ receive)
- 10-channel multiplexed ADC (support Maximum 500Ksamples/sec and 12-bit resolution)
- GPIO (up to 237 multi-functional input/ output ports)

General Description

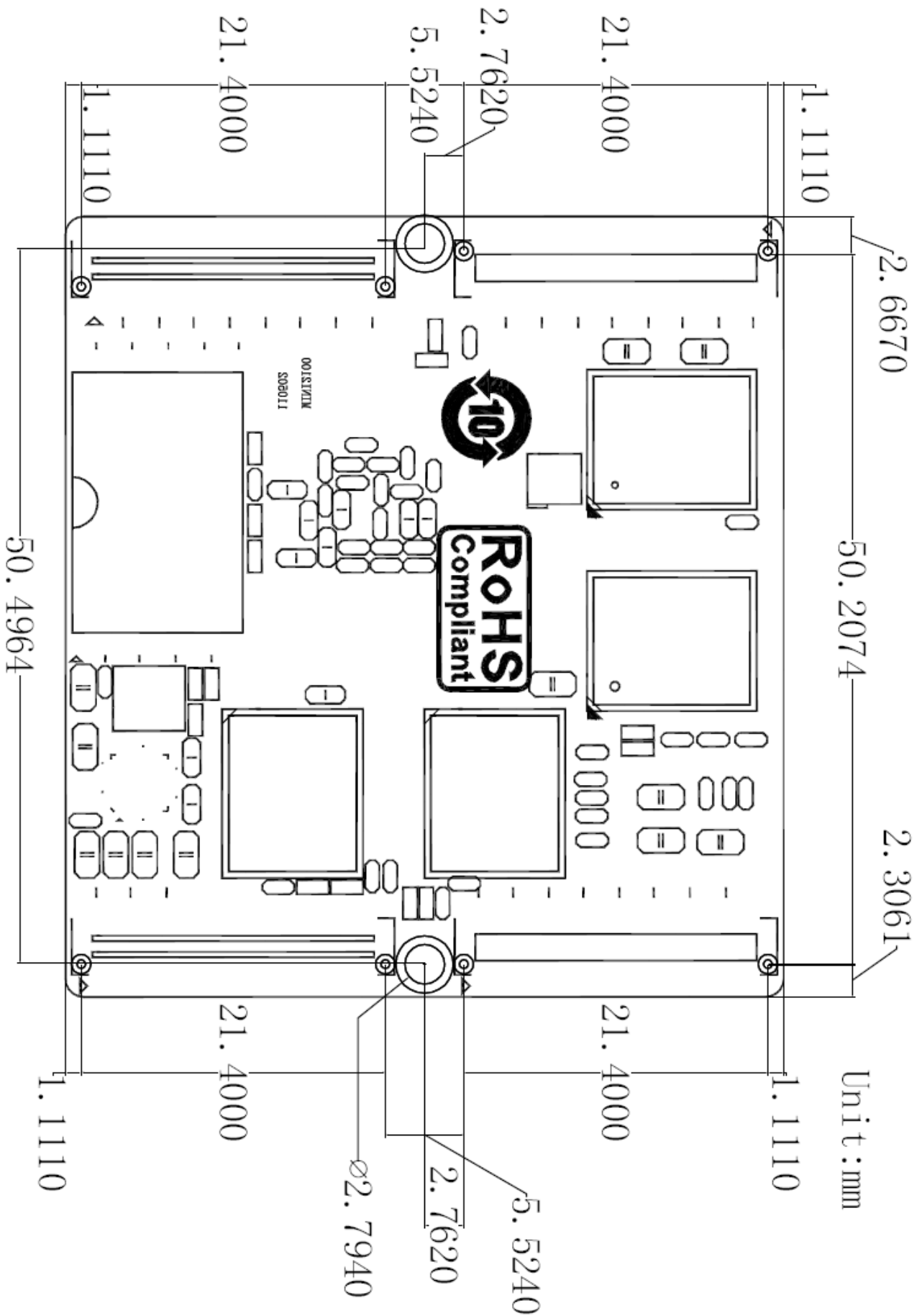
Embest Mini2100 processor card is based on Samsung's S5PV210 ARM Cortex-A8 application processor which is powered by 1GHz ARM Cortex-A8 core with built-in the programmable PowerVR SGX540 core. The board has 1Gbytes mobile DDR2 and 1Gbytes Nand Flash and uses four 0.5mm space 2*40-pin female board-to-board connectors to bring out many hardware peripheral signals and GPIOs from CPU.

The board is ideal for your next embedded design which you intend to use the S5PV210 for multi-media applications. Embest also designed an expansion board for integration of the Mini2100 processor card. The single board computer is called SBC2100. The board features 1080p HDMI and VGA/DVI-D video output which can implement large size monitor and TV display. The board is ready to run Android 2.2 and WinCE 6.0 operating systems and should be a solid platform for your design reference.

Functional Block Diagram



Dimensions



Mini2100 Bottom View

Four 2*40-pin Board-to-Board Female Expansion Connectors

Embest Mini2100 processor card is connected to carrier board via four 0.5mm space 2*40-pin board-to-board female connectors.

- The connector marked in red below is CN1, table 1-1 described the pin signals of CN1 connector.

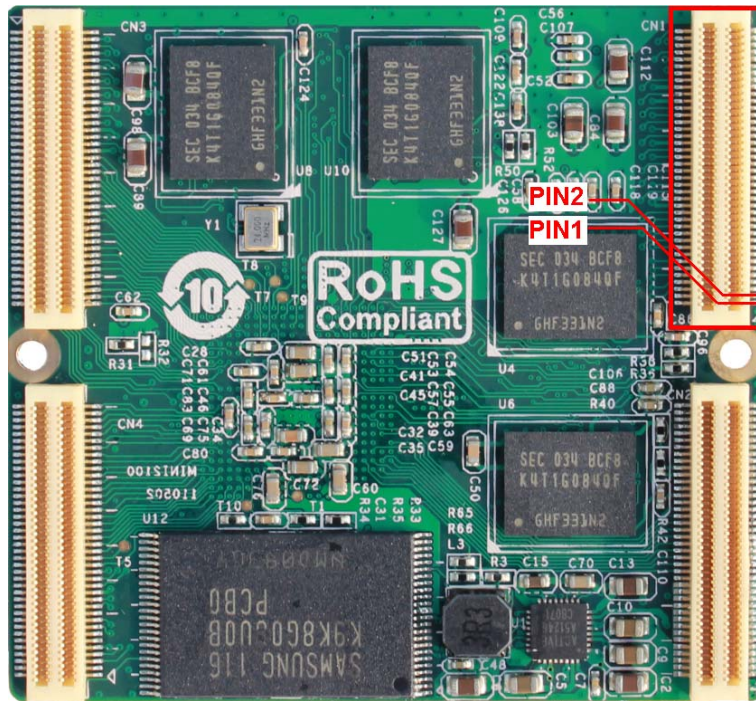


Table 1-1

CN1		
Pin	Signal	Description
1	XM0DATA1	Memory port 0 Data Bit 1
2	XM0DATA10	Memory port 0 Data Bit 10
3	XM0DATA13	Memory port 0 Data Bit 13
4	XM0DATA2	Memory port 0 Data Bit 2
5	XM0ADDR2	Memory port 0 Address Bit 2
6	USERLED33	SPI master output / slave input line for channel 0
7	GND	GND
8	GND	GND
9	GND	GND
10	GND	GND
11	L3DATA	SPI master input / slave output line for channel 0
12	CAM_B2_D3	Camera data bit 3
13	GND	GND
14	XMMC1CMD	COMMAND/RESPONSE (SD/ SDIO/ MMC card interface channel 1)
15	XMMC1DATA3	DATA3(SD/SDIO/MMC card interface channel 1)
16	XEINT23_HP_DECTECT	SD_3_DATA[2](SD/SDIO /MMC card interface channel 3)
17	GND	GND

18	XMMC0DATA0	DATA[0] (SD/ SDIO/ MMC card interface channel 0)
19	XMMC0DATA3	DATA[3] (SD/ SDIO/ MMC card interface channel 0)
20	CAM_B2_D7	Camera data bit 7
21	GND	GND
22	CAM_B2_HREF	MODEM (MSM) IF Address(MSM_ADDR[13] should be '0')
23	CAM_B2_FIELD	MODEM (MSM) IF Address(MSM_ADDR[13] should be '0')
24	CAM_B2_D4	Camera data bit 4
25	CAM_B2_VSYNC	MODEM (MSM) IF Address (MSM_ADDR[13] should be '0')
26	CAM_B2_D0	Camera data bit 0
27	CAM_B2_D5	Camera data bit 5
28	XM0DATA9	Memory port 0 Data Bit 9
29	GND	GND
30	XM0DATA11	Memory port 0 Data Bit 11
31	XM0DATA8	Memory port 0 Data Bit 8
32	GND	GND
33	GND	GND
34	GND	GND
35	GND	GND
36	VDD_MEM	+1.8V
37	VDD_MEM	+1.8V
38	VDD_MEM	+1.8V
39	VDD_MEM	+1.8V
40	VDD_MEM	+1.8V
41	XMMC3CDN	CARD DETECT (SD/SDIO/ MMC card interface channel 3)
42	L3MODE	SPI clock for channel 1
43	GPDB1_HDMI_I2C_EN	SPI chip select (only for slave mode) for channel 0
44	GPA1_2_3G_EN	SPI master input / slave output line for channel 1
45	GND	GND
46	GND	GND
47	GND	GND
48	CAM_B2_D1	Camera data bit 1
49	GND	GND
50	CAM_B2_D6	Camera data bit 6
51	GND	GND
52	CAM_B2_PCLK	XMSMADDR MODEM (MSM) IF Address (MSM_ADDR [13] should be '0')
53	CAM_B2_D2	Camera data bit 2
54	UART2_TX	UART2 Transit data
55	UART2_RX	UART2 Receive data
56	UART1_CTS	UART1 Clear To Send
57	GND	GND
58	UART2_CTS	UART2 Clear To Send
59	UART2_RTS	UART2 Request To Send
60	UART1_RTS	UART1 Request To Send
61	UART1_TX	UART1 Transit data
62	UART1_RX	UART1 Receive data

63	XMMC0CLK	CLOCK(SD/SDIO/MMC card interface channel 0)
64	XMMC0DATA1	DATA [1] (SD/ SDIO/ MMC card interface channel 0)
65	GND	GND
66	GND	GND
67	XMMC1CLK	CLOCK(SD/SDIO/MMC card interface channel 1)
68	XMMC1DATA2	DATA[2](SD/SDIO/MMC card interface channel 1)
69	SD2WP33	SPI clock for channel 0
70	XpwmTOUT2	PWM Timer Output
71	XpwmTOUT1	PWM Timer Output
72	XMMC3CLK	CLOCK(SD/SDIO/MMC card interface channel 3)
73	GND	GND
74	GPG1_0_MOTER	DATA[1] (SD/ SDIO/ MMC card interface channel 3)
75	XMMC3DATA3	DATA [3] (SD/ SDIO/ MMC card interface channel 3)
76	XMMC3DATA0	DATA [0] (SD/ SDIO/ MMC card interface channel 3)
77	GPA1_3_3G_RST	SPI master output / slave input line for channel 0
78	GPG1_7_3G_DIS	SPI chip select (only for slave mode) for channel 1
79	GND	GND
80	GND	GND

- The connector marked in red below is CN2, table 1-2 described the pin signals of CN2 connector.

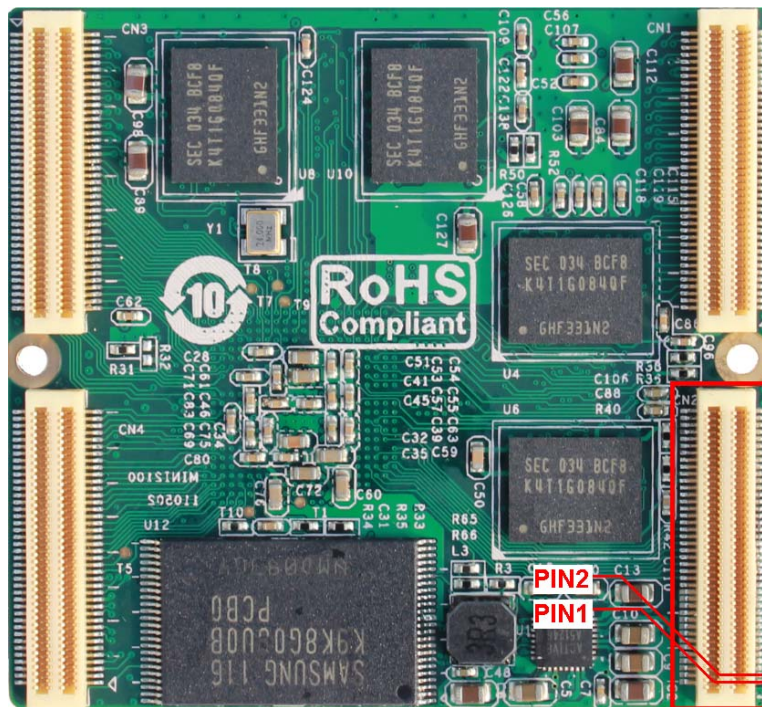


Table 1-2

CN2		
Pin	Signal	Description
1	VDD_REG1_IO	+3.3V
2	VDD_REG1_IO	+3.3V
3	VDD_REG1_IO	+3.3V
4	VDD_REG1_IO	+3.3V

5	VDD_REG1_IO	+3.3V
6	GND	GND
7	GND	GND
8	GND	GND
9	GND	GND
10	GND	GND
11	GND	GND
12	GND	GND
13	GND	GND
14	GND	GND
15	GND	GND
16	CAM_B2_CLKOUT	MODEM (MSM) IF Address(MSM_ADDR [13] should be '0')
17	GND	GND
18	GND	GND
19	GND	GND
20	GND	GND
21	GND	GND
22	VSYNC_LDI	GPIO
23	XjTCK	XjTCK (TAP Controller Clock) provides the clock input for the JTAG logic. Pull-down resistor is connected.
24	XI2CSDA0	IIC-bus clock for channel 0
25	XjTDI	XjTDI (TAP Controller Data Input) is the serial input for test instructions and data. Pull-up resistor is connected.
26	XjTMS	XjTMS (TAP Controller Mode Select) controls the sequence of the TAP Controller's states. Pull-up resistor is connected.
27	GND	GND
28	GND	GND
29	XadcAIN_4	ADC Analog Input Bit 4
30	GND	GND
31	XadcAIN_6	ADC Analog Input Bit 6
32	GND	GND
33	GND	GND
34	XadcAIN_7	ADC Analog Input Bit 7
35	XadcAIN_5	ADC Analog Input Bit 5
36	XM0DATA0	Memory port 0 Data Bit 0
37	XMMC2DATA3	DATA [3] (SD/ SDIO/ MMC card interface channel 2)
38	XMMC2CMD	COMMAND/RESPONSE (SD/ SDIO/ MMC card interface channel 2)
39	XMMC2DATA1	DATA [1] (SD/ SDIO/ MMC card interface channel 2)
40	XMMC2CLK	CLOCK (SD/ SDIO/ MMC card interface channel 2)
41	XM0DATA3	Memory port 0 Data Bit 3
42	XM0DATA12	Memory port 0 Data Bit 12
43	XM0DATA14	Memory port 0 Data Bit 14
44	XM0DATA7	Memory port 0 Data Bit 7
45	XjTRSTn	XjTRSTn (TAP Controller Reset) resets the TAP controller at start. If debugger (black ICE) is not used, XjTRSTn pin must be at L or low active pulse. Pull-down resistor is connected.

46	XM0DATA4	Memory port 0 Data Bit 4
47	XM0DATA5	Memory port 0 Data Bit 5
48	GND	GND
49	XM0WEN	Memory Port 0 SRAM / OneNAND Write Enable
50	GND	GND
51	GND	GND
52	XM0OEN	Memory Port 0 SRAM / OneNAND Output Enable
53	XM0CSN0	Memory Port 0 SRAM Chip select support up to 2 memory bank
54	GND	GND
55	XdacOUT	Analog output of DAC
56	XpwmTOUT3	PWM Timer Output
57	GPJ0_0_MOTER	COMMAND/RESPONSE (SD/ SDIO/ MMC card interface channel 3)
58	XI2CSCL0	IIC-bus data for channel 0
59	L3CLOCK	PWM Timer Output
60	XMMC1DATA0	DATA [0] (SD/ SDIO/ MMC card interface channel 1)
61	XMMC1CDN	CARD DETECT (SD/ SDIO/ MMC card interface channel 1)
62	XMMC1DATA1	DATA [1] (SD/ SDIO/ MMC card interface channel 1)
63	XMMC0DATA2	DATA [2] (SD/ SDIO/ MMC card interface channel 0)
64	XMMC0CMD	COMMAND/ RESPONSE (SD/ SDIO/ MMC card interface channel 0)
65	XMMC0CDN	CARD DETECT (SD/ SDIO/ MMC card interface channel 0)
66	NPBIN	Manual Reset
67	GND	GND
68	GND	GND
69	GND	GND
70	VDD_ALL	+5V
71	VDD_ALL	+5V
72	VDD_ALL	+5V
73	VDD_ALL	+5V
74	VDD_ALL	+5V
75	VDD_ALL	+5V
76	GND	GND
77	GND	GND
78	GND	GND
79	GND	GND
80	GND	GND

- The connector marked in red below is CN3, table 1-3 described the pin signals of CN3 connector.

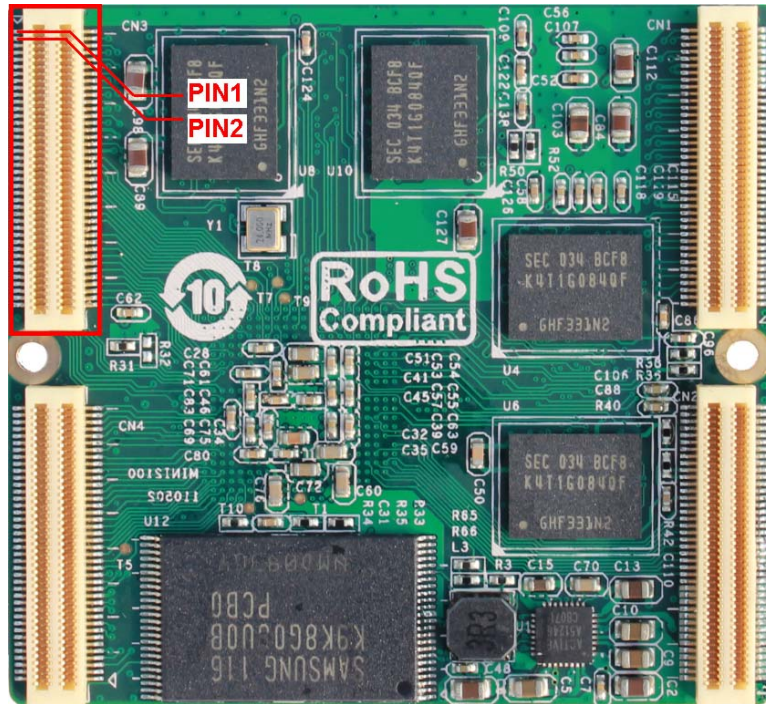


Table 1-3

CN3		
Pin	Signal	Description
1	VDD_RTC	+5V
2	VDD_RTC	+5V
3	DVI_IRQ	KeyIF_Column_data[4]
4	XUODRVVBUS	USB OTG charge pump enable
5	XEINT29_MENUKEY	GPIO
6	GND	GND
7	XEINT30_HOMEKEY	GPIO
8	XadcAIN_3	ADC Analog Input Bit 3
9	XadcAIN_0	ADC Analog Input Bit 0
10	XOM4	Boot strap pin
11	XOM5	Boot strap pin
12	XEINT1_NPBSTAT	External interrupt
13	XEINT5_CHR_FULL	External interrupt
14	XEINT3_VSEL	External interrupt
15	XEINT10_BACKKEY	Back Key
16	XEINT7_MENUKEY	Menu Key
17	XEINT12/HDMI_CEC	Consumer Electronics Control
18	XEINT14_GSENSOR_INT	External interrupt
19	HOTPLUG_DVI_IOn	DVI-D hot Plug Detect
20	CAM2_RST	External interrupt
21	XEINT24_KEY_UND	External interrupt
22	XEINT26_VOL-	External interrupt
23	XEINT13/HDMI_HPD	Hot plug and play detect

24	XEINT28	External interrupt
25	XCLKOUT	Clock out signal
26	XUHPWREN	USB HOST charge pump enable
27	XI2CSDA1	IIC serial bidirectional data
28	XI2CSCL1	IIC master serial clock
29	XI2CSCL2	IIC master serial clock
30	XUODP	USB Data+
31	XUODM	USB Data-
32	UART0_RX	UART0 Receive data
33	GND	GND
34	CAM_B_D1	Camera data bit 1
35	CAM_B_D0	Camera data bit 0
36	CAM_B_HREF	Horizontal Sync,driven by the Camera processor A.
37	CAM_B_VSYNC	Vertical Sync, driven by the Camera processor A.
38	GSO	KeyIF_Row_data[4]
39	XadcAIN_1	ADC Analog Input Bit 1
40	GSI	KeyIF_Row_data[3]
41	CAM_B_D7	Camera data bit 7
42	CAM_B_D6	Camera data bit 6
43	XUOVBUS	+5V
44	CAM_B_CLKOUT	Master Clock to the Camera processor A
45	CAM_B_D5	Camera data bit 5
46	CAM_B_FIELD	Specifies the Field signal driven by external Camera processor A
47	CAM_B_D3	Camera data bit 3
48	CAM_B_D2	Camera data bit 2
49	CAM_B_D4	Camera data bit 4
50	CAM_B_PCLK	Pixel Clock, driven by the Camera processor A
51	XEINT0_NIRQ	External interrupt
52	XEINT4_LCD_ON/OFF	NC
53	XEINT8_HOMEKEY	Home Key
54	XEINT0_PWRHOLD	External interrupt
55	NETINT33	Receive Clock
56	XOM2	Boot strap pin
57	XEINT9_CAP_TOUCH_RST	NC
58	XNRESET	System Reset
59	XnRSTOUT	For External device reset control
60	XOM1	Boot strap pin
61	XOM0	Boot strap pin
62	XnWRESET	System Warm Reset.
63	GND	GND
64	XEINT6_CHRING	External interrupt
65	CAM_RST	External interrupt
66	GND	GND
67	XEINT25_VOL+	External interrupt
68	XEINT31_BACKKEY	External interrupt

69	GND	GND
70	XEINT15_VBUS_DET	+3.2V
71	XEINT17_WLAN_EN	External interrupt
72	XEINT16_BT_EN	External interrupt
73	XEINT18_WLAN_IRQ	External interrupt
74	XOM3	Boot strap pin
75	GND	GND
76	XPWRRGTON	Power Regulator enable
77	XRTCCLKO	RTC Clock out
78	XEINT4_HUB_RST	KeyIF_Column_data[7]
79	XUHOVERCUR	USB HOST over current flag
80	XEINT27	External interrupt

- The connector marked in red below is CN4, table 1-4 described the pin signals of CN4 connector.

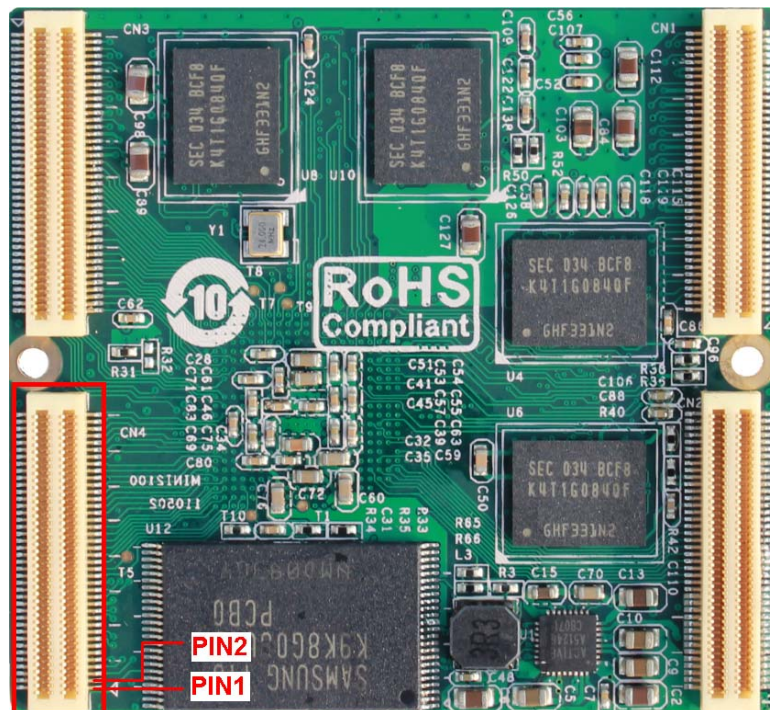


Table 1-4

CN4		
Pin	Signal	Description
1	VDD_1V8	+1.8V
2	VDD_1V8	+1.8V
3	XI2SSDO0_2	IIS-bus serial data output for channel 0 (Lower Power Audio)
4	XHDMIREXT	HDMI Phy Resistance
5	SYS_OE#	GPIO
6	GND	GND
7	GND	GND
8	XHDMITX0N	TMDS output data pair
9	XHDMITX0P	TMDS output data pair
10	GND	GND

11	XHDMITX2N	TMDS output data pair
12	XHDMITX2P	TMDS output data pair
13	GND	GND
14	XPCMEXTCLK0	PCM External Clock for channel 0
15	XEINT10_BACKKEY	External interrupt
16	XEINT7_MENUKEY	External interrupt
17	XMMC2DATA2	SD card data 2
18	XEINT14_GSENSOR_INT	External interrupt
19	XMMC2DATA0	SD card data 0
20	CAM2_RST	External interrupt
21	XI2SSDO0_1	IIS-bus serial data output for channel 0 (Lower Power Audio)
22	XMMC2CDN	Card Detect for SDMMC2
23	PCM_SOUT1_BT	IIS-bus serial data output for channel 1
24	PCM_SIN1_BT	IIS-bus serial data input for channel 1
25	XVVD20	LCD pixel data output for RGB interface
26	XVVD21	LCD pixel data output for RGB interface
27	XVVD19	LCD pixel data output for RGB interface
28	XVVD22	LCD pixel data output for RGB interface
29	XVVD5	LCD pixel data output for RGB interface
30	XVVD13	LCD pixel data output for RGB interface
31	XVVD3	LCD pixel data output for RGB interface
32	XVVD2	LCD pixel data output for RGB interface
33	XVVD8	LCD pixel data output for RGB interface
34	XVVD1	LCD pixel data output for RGB interface
35	XVVD0	LCD pixel data output for RGB interface
36	XVVDEN	Data Enable for RGB interface
37	XVCLK	Video Clock for RGB interface
38	XadcAIN_2	ADC Analog Input Bit 2
39	XadcAIN_8	ADC Analog Input Bit 8
40	XVHSYNC	Horizontal Sync Signal for RGB interface
41	XUHDP	USB HOST Data pin DATA(+)
42	XUHDM	USB HOST Data pin DATA(-)
43	XUOREXT	USB OTG External 44.2ohm (+/- 1%) resistor connection
44	HUHREXT	USB HOST External 44.2ohm (+/- 1%) resistor connection
45	XUOID	USB OTG Mini-Receptacle Identifier
46	XI2CSDA2	I2C-BUS Interface2 Serial Data Line
47	UART0_TX	UART0 Transit data
48	XadcAIN_9	ADC Analog Input Bit 9
49	XVVD7	LCD pixel data output for RGB interface
50	XVVD11	LCD pixel data output for RGB interface
51	XVVD6	LCD pixel data output for RGB interface
52	XVVD16	LCD pixel data output for RGB interface
53	XVVD10	LCD pixel data output for RGB interface
54	XVVD14	LCD pixel data output for RGB interface
55	XVVD15	LCD pixel data output for RGB interface
56	XVVD18	LCD pixel data output for RGB interface

57	XVVSYNC	Vertical Sync Signal for RGB interface
58	XVVD9	LCD pixel data output for RGB interface
59	XVVD4	LCD pixel data output for RGB interface
60	XVVD12	LCD pixel data output for RGB interface
61	XVVD23	LCD pixel data output for RGB interface
62	XVVD17	LCD pixel data output for RGB interface
63	XI2SLRCK0	IIS-bus channel select clock for channel 0 (Lower Power Audio)
64	XI2SSDO0_0	IIS-bus serial data output for channel 0 (Lower Power Audio)
65	XI2SSDI0	IIS-bus serial data input for channel 0 (Lower Power Audio)
66	XI2SCDCLK0	IIS CODEC system clock for channel 0 (Lower Power Audio)
67	XI2SSCLK0	IIS-bus serial clock for channel 0 (Lower Power Audio)
68	PCM_SCLK1_BT	IIS-bus serial clock for channel 1
69	PCM_FSYNC1_BT	IIS CODEC system clock for channel 1
70	XI2SSDO2_3G	PCM Serial Data Output for channel 0
71	XI2SSDI2_3G	PCM Serial Data Input for channel 0
72	GND	GND
73	XHDMITX1P	TMDS output data pair
74	XHDMITX1N	TMDS output data pair
75	GND	GND
76	XHDMITXCP	TMDS output clock pair -
77	XHDMITXCN	TMDS output clock pair +
78	GND	GND
79	XM0DATA15	Memory port 0 Data Bit 15
80	XM0DATA6	Memory port 0 Data Bit 6

Software Features

OS	Item	Remark	
Android	BIOS	x-loader	NAND / ONENAND
			MMC/SD
			FAT
		u-boot	NAND / ONENAND
			MMC/SD
			FAT
			NET
		Kernel	Android2.2
	File system	Ramdisk File System, UBI File System	
		udev support	
Driver	Nand Flash, SDRAM, HDMI, DVI-D, VGA, Serial port, Ethernet, USB OTG, USB EHCI, SD card, Audio input/output, Key, LED, RTC (in source code)		
	2D/3D (library file, no source code provided)		
Application Demo	MP3/MPEG4/H264 DSP hardware decoder (library file, no source code provided)		
Cross-compile toolchains	arm-eabi-4.4.0+arm-2009q3-67-arm-none-linux-gnueabi-i686-pc-linux-gnu		
WinCE	Steploader	UART	
		NAND	
		MMC/SD	
	Eboot (WinCE6.0)	UART	
		NAND	
		MMC/SD	
	OAL (in source code)	KILT (USB RNDIS & USB serial), Boot parameter, RTC, System timer, Interrupt controller, MMU, Serial Debug Port, Kernel Profiler-use timer2, Library Abstrations (GPIO abstrations), Power management	
	Driver (in source code)	Audio (I2S and AC97), Backlight, Battery, Camera, CEC, CMM (codec memory management), Display, I2C, IROM BOOT, JTAG, Keypad, MFC (Mutli-Format Codec, MPEG2,MPEG4, H.263,H.264, VC-1), Nand Flash, NLED, OTG Device, Power Button, Power Control, SD/MMC, Serial port, SPI, Touch Screen, TVOUT(HDMI and Composite Video), USB EHCI, USB OHCI, DM9000 NDIS, CH7033 (DVI/VGA)	
	Application Demo (in source code)	GPIO application demo and HDMI output example	
	Software features	Supports .NET Compact Framework 3.5 and KITL kernel debug	
Supports Hive registry and ROM file system			

Order Information

Order No.	T400302
Item	Embest Mini2100 Processor Card
Options	Embest SBC2100 Single Board Computer
Price	Please contact Embest



Embest Info&Tech Co., LTD.

Room 509, Luohu Science&Technology Building,
#85 Taining Rd., Shenzhen, Guangdong, China 518020

Tel: +86-755-25635656/25636285

Fax: +86-755-25616057

Email: market@embedinfo.com

<http://www.embedinfo.com/english>

<http://www.armkits.com>